What is claimed is:

1. A level shift circuit, comprising:

a first conduction type first transistor wherein a first power source voltage is supplied to a source, a first input signal is applied to a gate, and a first terminal is connected to a drain;

a first conduction type second transistor wherein a second input signal in reverse relation to the first input signal is applied to a gate, and a drain is connected to a second terminal;

a second conduction type third transistor wherein a second power source voltage is supplied to a source, and the first terminal is connected to a drain;

a second conduction type fourth transistor wherein the second terminal is connected to a drain;

a first gate voltage control circuit connected to the second terminal, input the second input signal, and making said third transistor turen ON when said first transistor is OFF; and

a second gate voltage control circuit connected to the first terminal, input the first input signal, and making said fourth transistor turen ON when said second transistor is OFF.

2. The level shift circuit of claim 1,

wherein said first gate voltage control circuit comprises:

a first conduction type fifth transistor in which the first power source voltage is supplied to a source, a gate of said third transistor is connected to a drain, and the second input signal is applied to a gate; and

a second conduction type sixth transistor in which the second terminal is connected to a source, and the gate of said third transistor is connected to a gate and a drain,

wherein said second gate voltage control circuit comprises:

a first conduction type seventh transistor in which the first power source voltage is supplied to a source, a gate of said fourth transistor is connected to a drain, and the first input signal is applied to a gate; and

a second conduction type eighth transistor in which the first terminal is connected to a source, and the gate of said fourth transistor is connected to a gate and a drain.

3. The level shift circuit of the claim 2,

wherein said first gate voltage control circuit further comprises a second conduction type ninth transistor in which the second terminal is connected to a source, the gate of said third transistor is connected to a drain, and the second input signal is applied to a gate, and

wherein said second gate voltage control circuit further comprises a second conduction type tenth transistor in which the first terminal is connected to a source, the gate of said fourth transistor is connected to a drain, and the first input signal is applied to a gate.

4. The level shift circuit of the claim 1,

wherein said first gate voltage control circuit comprises:

a first conduction type fifth transistor in which the first power source voltage is supplied to a source, the gate of the third transistor is connected to a drain, and the second input signal is applied to a gate; and a second conduction type eleventh transistor in which the second terminal is connected to a source, the gate of the third transistor is connected to a gate and a drain, and a current flows between the source and the drain even when a gate-source voltage is 0V,

wherein said second gate voltage control circuit comprises:

a first conduction type seventh transistor in which the first power source voltage is supplied to a source, the gate of the fourth transistor is connected to a drain, and the first input signal is applied to a gate; and

a second conduction type twelfth transistor in which the first terminal is connected to a source, and the gate of the fourth transistor is connected to a gate and a drain, and a current flows between the source and the drain even when a gate-source voltage is 0V.

5. The level shift circuit of claim 1, further comprising:

a first switching circuit connected in series relation to said first transistor between the first terminal and the first power source, controlled by a gate voltage of said third transistor, and having a switching means which turns ON when said third transistor is OFF; and

a second switching circuit connected in series relation to said second transistor between the second terminal and the first power source, controlled by a gate voltage of said fourth transistor, and having a switching means which turns ON when said fourth transistor is OFF.

6. The level shift circuit of claim 1, further comprising:

a third switching circuit connected in series relation to said first transistor between the first terminal and the first power source, controlled by a voltage of the second terminal, and having a switching means which turns OFF when a voltage of the second terminal is at same voltage level as the first power source voltage; and

a fourth switching circuit connected in series relation to said second transistor between the second terminal and the first power source, controlled by a voltage of the first terminal, and having a switching means which turns OFF when a voltage of the first terminal is at same voltage level as the first power source voltage.

7. A level shift circuit, comprising:

a first conduction type second transistor wherein a first power source voltage is supplied to a source, a second input signal in reverse relation to a first input signal is applied to a gate, and a drain is connected to a second terminal;

a second conduction type fourth transistor wherein a second power source voltage is supplied to a source, and the second terminal is connected to a drain;

a second conduction type thirteenth transistor wherein the second power source voltage is supplied to a source;

a third gate voltage control circuit connected to the second terminal, input the second input signal, and making said thirteenth transistor turen ON when the second input signal is at a high level; and

a fourth gate voltage control circuit connected to a drain of said thirteenth transistor, input the first input signal, and making said fourth transistor turen ON when the first input signal is at a high level.

8. The level shift circuit of claim 7, further comprising:

a second switching circuit connected in series relation to said second transistor between the second terminal and the first power source, and also connected to a gate of said fourth transistor.

9. The level shift circuit of claim 7, further comprising:

a fourth switching circuit connected in series relation to said second transistor between the second terminal and the first power source, and also connected to a drain of said thirteenth transistor.